PATENT COOPERATION TREA

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Assistant Commissioner for Patents
United States Patent and Trademark Office
Box PCT
Washington, D.C.20231
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing (day/month/year) 18 July 2000 (18.07.00)	
International application No. PCT/GB99/03776	**Applicant's or agent's file reference** 4/W32292WO
International filing date (day/month/year) 12 November 1999 (12.11.99)	**Priority date** (day/month/year) 13 November 1998 (13.11.98)
Applicant UNDERHILL, Michael, James	

1. The designated Office is hereby notified of its election made:

[X] in the demand filed with the International Preliminary Examining Authority on:

09 June 2000 (09.06.00)

[ ] in a notice effecting later election filed with the International Bureau on:

2. The election [X] was

[ ] was not

made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO **34, chemin des Colombettes** **1211 Geneva 20, Switzerland**	Authorized officer Pascal Piriou
Facsimile No.: (41-22) 740.14.35	Telephone No.: (41-22) 338.83.38

Form PCT/IB/331 (July 1992)

GB9903776

PATENT COOPERATION TREATY

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INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	FOR FURTHER ACTION	see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.
4/W32292WO		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/GB 99/ 03776	12/11/1999	13/11/1998
Applicant		
UNIVERSITY OF SURREY et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

[ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

[ ] contained in the international application in written form.

[ ] filed together with the international application in computer readable form.

[ ] furnished subsequently to this Authority in written form.

[ ] furnished subsequently to this Authority in computer readble form.

[ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

[ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

[X] the text is approved as submitted by the applicant.

[ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

[X] the text is approved as submitted by the applicant.

[ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 6

[ ] as suggested by the applicant.

[ ] because the applicant failed to suggest a figure.

[X] because this figure better characterizes the invention.

[ ] None of the figures.

INTERNATIONAL SEARCH REPORT

[redacted]ational Application No
PCT/GB 99/03776

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K5/1252 H03K5/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 071 781 A (KAYALIOGLU INANC) 31 January 1978 (1978-01-31) column 2, line 4-54; figure 1	1
X	EP 0 592 048 A (EASTMAN KODAK CO) 13 April 1994 (1994-04-13) figure 10	1
A	EP 0 383 271 A (TOKO INC) 22 August 1990 (1990-08-22) figure 1	1
A	KRAUS K: "FAST DC-COUPLED TRIGGER" ELECTRONICS WORLD AND WIRELESS WORLD,GB,REED BUSINESS PUBLISHING, SUTTON, SURREY, vol. 96, no. 1651, page 7 XP000123343 ISSN: 0959-8332	1,26

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 January 2000	02/02/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Moll, P

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 99/03776

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 438 289 A (KAN RIKIYA ET AL) 1 August 1995 (1995-08-01) column 4, line 20 -column 5, line 58; figures 1-3	1,19
A	US 4 142 110 A (WEBER RUDOLF) 27 February 1979 (1979-02-27) column 2, line 20 -column 3, line 15; figure 2	1-6
A	PATENT ABSTRACTS OF JAPAN vol. 007, no. 062 (E-164), 15 March 1983 (1983-03-15) & JP 57 207419 A (ORIENT TOKEI KK), 20 December 1982 (1982-12-20) abstract	1,13

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 99/03776

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4071781 A	31-01-1978	NONE	
EP 0592048 A	13-04-1994	US 5461223 A	24-10-1995
		CA 2106715 A,C	10-04-1994
		JP 6215167 A	05-08-1994
		US 5536929 A	16-07-1996
		US 5536927 A	16-07-1996
		US 5548109 A	20-08-1996
		US 5528023 A	18-06-1996
EP 0383271 A	22-08-1990	JP 2215221 A	28-08-1990
		JP 2707461 B	28-01-1998
		DE 69024981 D	07-03-1996
		DE 69024981 T	12-09-1996
		US 5175748 A	29-12-1992
US 5438289 A	01-08-1995	JP 2597342 B	02-04-1997
		JP 6167517 A	14-06-1994
US 4142110 A	27-02-1979	NONE	
JP 57207419 A	20-12-1982	NONE	

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
4/W32292WO		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/GB99/03776	12/11/1999	13/11/1998
International Patent Classification (IPC) or national classification and IPC H03K5/1252		
Applicant UNIVERSITY OF SURREY et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   ☐ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☒ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☐ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
09/06/2000	12.03.2001
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Moll, P Telephone No. +49 89 2399 2197

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/GB99/03776

I. Basis of the r p rt

1. This report has been drawn on the basis of *(substitute sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to the report since they do not contain amendments (Rules 70.16 and 70.17).)*:
Description, pages:

1-15 as originally filed

Claims, No.:

1-28 as originally filed

Drawings, sheets:

1/10-10/10 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

III. Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

1. The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non-obvious), or to be industrially applicable have not been examined in respect of:

☐ the entire international application.

☒ claims Nos. 28.

because:

☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international preliminary examination (*specify*):

☒ the description, claims or drawings (*indicate particular elements below*) or said claims Nos. 28 are so unclear that no meaningful opinion could be formed (*specify*):
see separate sheet

☐ the claims, or said claims Nos. are so inadequately supported by the description that no meaningful opinion could be formed.

☐ no international search report has been established for the said claims Nos. .

2. A meaningful international preliminary examination report cannot be carried out due to the failure of the nucleotide and/or amino acid sequence listing to comply with the standard provided for in Annex C of the Administrative Instructions:

☐ the written form has not been furnished or does not comply with the standard.

☐ the computer readable form has not been furnished or does not comply with the standard.

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N) Yes: Claims 1-27

	No:	Claims	
Inventive step (IS)	Yes:	Claims	1-27
	No:	Claims	
Industrial applicability (IA)	Yes:	Claims	1-27
	No:	Claims	

2. Citations and explanations
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

R It ms III and VIII

1). Claim 28 contains a reference to the drawings. According to Rule 6.2(a) PCT, claims should not contain such references except where absolutely necessary, which is not the case here. Claim 28 is therefore unclear and cannot be examined as to novelty, inventive step or industrial applicability.

2). Claim 1 introduces an integrator charge storage means on which a time varying voltage waveform is created. Said time varying voltage waveform is indicated to have a mean d.c. voltage level. Some means are defined for comparing the said time varying voltage waveform with said mean d.c. voltage level. The latter step, however, requires the mean d.c. voltage level to be actually available as a signal that can be applied to the means for comparing. Claim 1 is, however, silent as to how the said mean d.c. voltage level is eventually created. It is clear from the description on pages 4, lines 8-11 from below that the following feature is essential to the definition of the invention:

"a high impedance low pass filter (R1, C4) connected to the integrator storage capacitor (C3) establishes the mean d.c. voltage level".

It is noted that this circuit detail is consistently depicted in the present drawings Figures 2(a), 4(a), 5(a), 6, 7(a), 8(a) and 9(a).

Since independent claim 1 does not contain this feature it does not meet the requirement following from Article 6 PCT taken in combination with Rule 6.3(b) PCT that any independent claim must contain all the technical features essential to the definition of the invention. For the purposes of this report it is, under section V, proceeded on the assumption that claim was clarified along the lines set forth above.

3). For the sake of completeness it is stressed that the vague language of present claim 1 would permit the claim to be even read in a novelty-destroying manner onto prior art document US-A-4 071 781, note the integrator charge storage

means (16), the mean d.c. voltage level (at D) and the means for comparing (10) in Figure 1 of the said document, cf. also the signals "PULSES AT B" and "AVERAGE VOLTAGE AT D" in Figure 2. The fact that document US-A-4 071 781 anticipates the features of present claim 1 although the basic concept underlying the invention differs substantially from the known circuit (the circuitry for creating the mean d.c. voltage level is connected to the integrator storage capacitor, rather than directly to the input as in the prior art) makes it quite plain that the scope of claim 1 is broader than justified by the description and drawings. Claim 1 is therefore not supported by the description as required by Article 6 PCT.

4). The embodiment of the invention shown in figure 10 does not fall within the scope of the claims, as there is, in Figure 10, no means for comparing within the meaning of claim 1. This inconsistency between the claims and the description leads to doubt concerning the matter for which protection is sought, thereby rendering the claims unclear (Article 6 PCT).

Re Item V

The present invention relates to an anti-jitter circuit in an input pulse train. Closest prior art is reflected by document US-A-4 071 781.

Were claim 1 clarified as indicated above under item 2), the subject-matter of the claim would be distinguished over the cited prior art in that the circuitry for creating the mean d.c. voltage level is connected, according to the invention, to the integrator storage capacitor rather than directly to the input as in the prior art. This modification appears to improve performance of the circuitry in that accuracy of level comparison is increased. There being nothing in the available prior art to suggest this, the subject-matter of such claim would be found to be novel and inventive, Articles 33(2)(3) PCT. Industrial applicability is obviously not in doubt.

Claims 2-27 are dependent claims within the meaning of Rule 6.4 PCT. They are directed to particular embodiments of the anti-jitter circuit set forth in claim 1.

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H03K 5/1252, 5/08 — A1

(11) International Publication Number: **WO 00/30256**

(43) International Publication Date: 25 May 2000 (25.05.00)

(21) International Application Number: PCT/GB99/03776

(22) International Filing Date: 12 November 1999 (12.11.99)

(30) Priority Data:
9824989.9 13 November 1998 (13.11.98) GB
9907733.1 1 April 1999 (01.04.99) GB

(71) Applicant *(for all designated States except US)*: UNIVERSITY OF SURREY [GB/GB]; Guildford, Surrey GU2 5XH (GB).

(72) Inventor; and

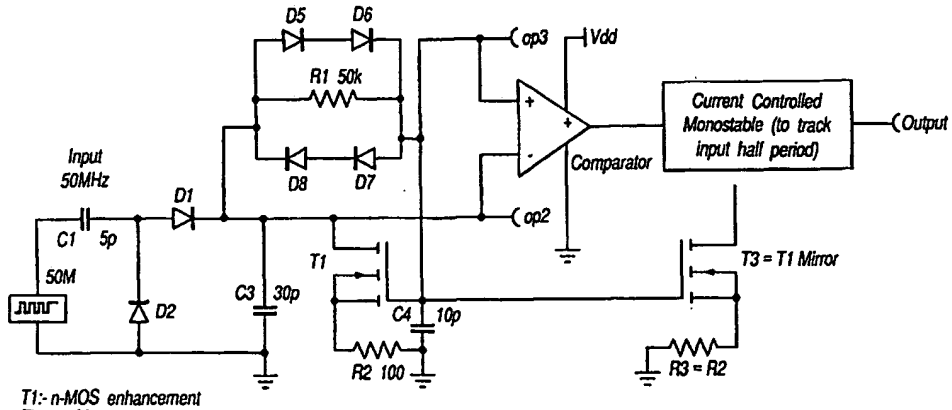
(75) Inventor/Applicant *(for US only)*: UNDERHILL, Michael, James [GB/GB]; Hatchgate, Tandridge Lane, Lingfield, Surrey RH7 6LL (GB).

(74) Agent: MATHISEN, MACARA & CO.; The Coach House, 6–8 Swakeleys Road, Ickenham, Uxbridge UB10 8BZ (GB).

(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
With international search report.

(54) Title: ANTI-JITTER CIRCUITS



T1:- n-MOS enhancement Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

AAJC with Comparator and input-tracking Output Monostable

(57) Abstract

An anti-jitter circuit has an integrator storage capacitor (C3). A charge pump (C1, D1, D2) derives from an input pulse train at least one charge packet during each cycle of the input pulse train and supplies the charge packets to the storage capacitor (C3). A controlled current sink (T1) operating in conjunction with a high impedance low pass filter (R1, C4) continuously discharges the storage capacitor (C3) to create a sawtooth voltage waveform (Op2) having a mean d.c. voltage level (Op3). A differential comparator compares the sawtooth voltage waveform (Op2) with the mean d.c. voltage level (Op3) and the comparator output is used to trigger a monostable circuit to generate an output pulse train having reduced time jitter.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
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DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

ANTI-JITTER CIRCUITS

FIELD OF THE INVENTION

This invention relates to anti-jitter circuits (AJC).

BACKGROUND OF THE INVENTION

An AJC is described in our European patent application No. 97903456.8 based on International patent application, publication No. WO 97/30516. The described AJC circuit provides a unique way of reducing phase noise or time jitter on a frequency source, typically 20 dB or more for the or each (fully cascaded) stage. Figures 1(a) to 1(c) of the accompanying drawings illustrate the principle of operation of this earlier AJC. Figure 1(a) is a block circuit diagram of the system described in the earlier patent application, Figure 1(b) shows an input pulse train with jitter (shown in broken outline) on the central pulse and Figure 1(c) shows the corresponding integrator output (Op2) and the comparator switching level (Op3).

The present invention provides an improvement over this earlier AJC. Because the implementation of the core part of the improved AJC requires no d.c. power the term adiabatic anti-jitter circuit (AAJC) will be used hereinafter.

SUMMARY OF THE INVENTION

According to the invention there is provided an anti-jitter circuit for reducing time jitter in an input pulse train comprising:

an integrator charge storage means,

charging means for deriving from the input pulse train at least one charge packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means, and

discharging means for continuously discharging the integrator charge storage means,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage waveform having a mean d.c. voltage level, and

means for comparing said time varying voltage waveform with said mean d.c. voltage level and deriving an output pulse train as a result of the comparison.

DESCRIPTION OF THE DRAWINGS

Anti-jitter circuits according to the invention are now described, by way of example only, with reference to the accompanying drawings in which:

Figures 1(a) to 1(c) illustrate a known anti-jitter circuit described in our International patent application, publication number WO 97/30516,

Figures 2(a) to 2(d) illustrate an embodiment of an anti-jitter circuit according to the present invention. Figure 2(a) is a circuit diagram of the anti-jitter circuit. Figure 2(b) shows an input waveform Op1, a sawtooth waveform Op2 and a mean d.c. level Op3. Figure 2(c) shows the waveforms Op2 and Op3 superposed and Figure 2(d) shows a detail of the superposed waveforms,

Figures 3(a), 3(b); 4(a), 4(b) and 5(a), 5(b) illustrate further embodiments of the anti-jitter circuit shown in Figures 2(a) to 2(d). Figures 3(a), 4(a) and 5(a) are circuit diagrams showing the anti-jitter circuits and Figures 3(b), 4(b) and 5(b) show the respective sawtooth waveforms Op2 and the mean d.c. levels Op3 overlaid.

Figure 6 shows an anti-jitter circuit according to the invention in which the pulse length of an output monostable circuit is controlled,

Figures 7(a) to 7(c) show an anti-jitter circuit according to the invention having a frequency doubling input. Figure 7(a) is a circuit diagram of the anti-jitter circuit. Figure 7(b) shows the sawtooth waveform Op2 and the mean d.c. level Op3 overlaid and Figure 7(c) shows an expanded detail of the overlaid waveforms.

Figures 8 and 9 show anti-jitter circuits according to the invention including circuitry arranged to maintain the charge value of charge packets substantially constant. Figures 8(a) and 9(a) are circuit diagrams showing the anti-jitter circuits. Figures 8(b)

and 9(b) show the input waveforms Op2 and the mean d.c. levels Op3 overlaid, and Figures 8(c) and 9(c) show an expanded detail of the overlaid waveforms. Figures 8(b) and 8(c) also show a voltage waveform Op4, and

Figure 10 shows a further embodiment of an anti-jitter circuit according to the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

The principle of operation can be seen by reference to Figures 2a to 2d, and it has some similarities to that of a charge pump. An approximately constant charge packet is formed either once or, in a second variation of the scheme, twice per input frequency source cycle. Each charge packet adds to the charge in an integrator storage capacitor C3. A controlled current source T1 (or more accurately current sink) discharges the capacitor C3 at a rate that maintains a substantially constant mean dc voltage level on the integrator storage capacitor C3. A high impedance low pass filter (R1, C4) connected to the integrator storage capacitor C3 establishes the mean d.c. voltage level that then controls the discharge current in a negative feedback configuration. The combination of intermittent charging and continuous discharging creates a sawtooth voltage waveform Op2 on the integrator storage capacitor C3. The two (high impedance) inputs of a differential comparator (not shown) are connected respectively to the input and output of the low pass filter. This establishes switching points when the mean dc level Op3 is equal to the sawtooth voltage waveform Op2

present on the integrator storage capacitor C3. The switching point on the discharge part of the sawtooth waveform has very much reduced timing jitter (as described in the aforementioned publication). This discharge switching transition then triggers an output monostable or divide-by-two circuit, as described in that publication.

The combination of the negative feedback and the differential comparator means that the correct comparator switching levels are established automatically for a very wide range of input frequencies without any change of circuit components values.

When the (optional) diodes D5 to D8 in Fig 2 are not conducting, the time constant R1C3C4/(C3+C4) determines the sideband frequency below which the jitter suppression starts to degrade at a 6dB per octave rate. The optimum loop gain is found to be $gmR1 = (C3+C4)^2/C3C4$. For a FET we have $gm = \sqrt{(2I_{dis}\beta)}$ and from the explanation below it can be seen that $I_{dis}=f_{ina}Q$, that is proportional to input frequency. The consequence is that the loop gain varies as the square root of input frequency. For such a control loop the loop gain can typically be allowed to vary by up to four to one with little variation in overall settling time or loop bandwidth. This then corresponds to a working frequency range of sixteen to one with no changes in component values.

The four optional "speed up" diodes D5 to D8 shown across the resistor R1 provide a low impedance path from input to the output shunt capacitor C4 of the low pass filter if the positive or negative voltage exceeds 2 diode (Vbe) offset levels

(approximately 2 x 0.6 volts typically). This option lowers the time constant of the low pass filter by orders of magnitude during initial acquisition of lock of output signal to input signal, or if large frequency or phase jump deviations occur in the input signal. The time for initial acquisition is thus much reduced and input to output lock is maintained (with no input pulses missed) over a wider range of input deviations of phase or frequency. The presence of the diodes also allows phase jitter sideband components much closer to carrier to be better suppressed after a full settling has occurred.

In the case of the charge pump arrangement of diodes D1 and D2, and input capacitor C1 in Fig 2(a), the peak-to-peak amplitude V_{ppst} of the sawtooth waveform is given approximately by the relationship $Q = C_3 V_{ppst} = C_1 V_{ppin}$, where V_{ppin} is the peak-to-peak input voltage and C_3 is the integrator storage capacitance. Q is actually the quantity of charge being transferred from C1 to C3 each time a transfer occurs. A large phase jitter adds substantially to the peak-to-peak voltage swing whilst two diode offsets should be subtracted from V_{ppin} to obtain a more accurate relationship. This relationship is used to ensure that the worst case V_{ppst} for the sawtooth is sufficiently less than 4 (Vbe) diode offsets range between the switch on levels of the speed up diodes D5 to D8.

Conveniently, controlled current source T1 is a transistor in the form of an insulated gate FET (as shown in Fig 2(a)). Alternatively a high input impedance bipolar

transistor combination such as a Darlington arrangement may be used in place of T1. A high input impedance is desirable so that a long time constant (or low cut off frequency) can be obtained for the low pass filter and at the same time keeping the value of the filter capacitor C4 to a low value. For fastest speed up acquisition time, C4 is made comparable in value to charge pump and storage capacitors C1 and C3.

The mean diode discharge current I_{dis} is given by the relationship $I_{dis} = f_{ina} Q$ where the charge packet Q has been defined in the above and f_{ina} is the rate of input frequency active transitions. Thus the FET or transistor characteristics should be chosen to provide this current at the desired mean sawtooth voltage. The value of the resistor R2 can also be conveniently chosen to reach this desired design objective; particularly there is a constraint on the choice of transistor characteristics. For a given transistor choice the resistor R2 can also be conveniently chosen to give a typical 10 to 1 operating frequency range anywhere within a design envelope of typically 1000 to 1, without having to alter the value of any other component within the circuit.

Figs 3 and 4 demonstrate by simulation the extreme frequency range limits of the AAJC shown in Figure 2 when only the resistor R2 is varied. However, purely for the purpose of display of aquisition within a limited number of input waveform cycles, the time constant C4R1 has been appropriately chosen in each case. Fig 5 shows the AAJC simulation operating of 5GHz. In all cases the waveforms are for operation starting from initial switch on. The acquisition time is when the two waveforms of

Op2 and Op3 intersect with no further missed intersections.

As an additional improvement, shown in Figure 6, the mean dc output from the low pass filter (being a direct function of may be frequency) can be used directly or through a matched current mirror process to control the pulse length of an output monostable. In this way the overall circuit can be made self-adjusting in terms of maintaining a good output waveform mark space ratio over a wide frequency range. A circuit arrangement for this is regarded as existing state of the art.

All the power for the AAJC circuit is obtained from the input source. An approximate estimate for the power dissipated in the circuit is the product of the discharge current and the mean d.c. voltage. Given ideal components there are no other dissipative processes in the circuit. A safer limit allowing for other losses would be to take the product of the input voltage swing and the discharge current.

A typical AAJC would operate with a discharge current of less than 1 to 2mA with a 5 volt input swing. In this example the input source would have to provide a maximum of 10mW.

In addition it is advantageous if the source waveform rise and fall times are short. Times of less than about one tenth of an average period minimise potential amplitude to phase conversion of any noise appearing at the input.

The amplitude of the input waveform should be reasonably constant over the short term. However it is a feature of the circuit that it automatically adjusts for long term (low frequency) variations in the input amplitude.

A frequency doubling circuit can be implemented in a very simple way with the AAJC as shown in Figures 7, 8 and 9. Here there are two input charge pumps C1, D1; C2, D2 which operate alternately on the rising and falling edges of the input waveform. The transformer XMR, is shown by way of example only and may be replaced by some transformerless push pull active circuit operating on the input signal. Advantages of frequency doubling and then dividing to obtain the final output are a further 6dB of phase noise reduction and an equal output mark space ratio which is retained over the whole frequency range of operation.

A disadvantage of the simple diode charge pump as shown is that the value of the charge packets is approximately proportional to the voltage existing on the integrator storage capacitor at the start time of the charge packets. Thus to obtain the best jitter reduction it is advisable to keep the peak-to-peak sawtooth voltage as a small percentage as possible of the mean voltage. Figs 8 and 9 show a frequency doubling circuit where the charge packets are kept much more constant by the presence of transistor T2 and its base components C5 and R3 which perform an averaging function over a few input cycles. The transistor operates essentially in the grounded base mode while conveying charge. Since the base voltage stays constant over several input

cycles any phase jumps causing the mean level of the sawtooth waveform to vary do not cause the size of the charge packets to vary. The input capacitors C1 and C2 are charged or discharged into constant voltage sinks. Obviously this technique also applies to the basic circuits as well where frequency doubling is not implemented.

Fig 9 shows a more convenient arrangement if T2 is a FET. The time constant components C5 and R3 are no longer required because the gate of T2 is connected to the gate of T1.

Transistors T2 in Fig 8 and Fig 9 are the most likely devices to restrict the upper frequency operation of the circuit. Because the mobility of holes is less than for electrons it may be advantageous to exchange p-devices for n-devices (or pnp for npn) and vice versa and at the same time reverse the sense of the input diodes. It is likely in practice that this will result in somewhat higher maximum frequency of operation.

In the embodiments described with reference to Figures 2 to 9 the sawtooth waveform (Op2) and the mean d.c level (Op3) are supplied to respective inputs of a differential comparator.

It will be appreciated that a DC reference point in these circuits may conveniently be chosen to be at any RF ground point because points connected by low frequency capacitors or decoupling capacitors are effectively all at the same RF potential.

Therefore, the ground connection in the embodiments of Figures 2 to 9 could be replaced by a suitably decoupled low impedance voltage source connected to the gate of the FET (or the base of an equivalent bipolar transistor). This voltage source can be arranged to establish the correct switching level for the comparator, which then can be a simple single input comparator, such as a high impedance CMOS inverter (NOT gate) instead of the differential comparator used in the embodiments of Figures 2 to 9.

Figure 10 shows a further embodiment of the invention in which a NOT gate U4 is used as a fast switching comparator. The switching level of the gate can vary appreciably with time and temperature; however, this can be controlled by provision of a further negative DC feedback path connected between the output of NOT gate U4 and the control input i.e. the gate of FET Q1. To this end, a simple, single RC low pass filter (R_5,C_5) provides sufficient filtering to establish the mean output level. In this way, the NOT gate U4 is automatically 'self-biased' to the correct switching level.

As in the embodiments of Figures 2 to 9, the input source V1 is connected to isolating capacitor C1 and to diodes D1,D2 which feed pulses to the integrator storage capacitor C3. FET Q1 discharges the capacitor C3 and the resultant sawtooth waveform is supplied to the comparator; that is, to the single input of the NOT gate U4.

The NOT gate U4 feeds the RC low pass filter R5,C5 which produces a mean DC

voltage level on capacitor C5 and this voltage is supplied to the gate of FET Q1 as an offset reference voltage. As before, FET Q1 in combination with resistor R1 acts as a current drain and the voltage on capacitor C4 governs the voltage on resistor R1 and hence the constant current discharging capacitor C3 via resistor R1.

As before, R2 is a large value resistor which in combination with capacitors C3 and C4 establishes the sideband frequency below which the jitter suppression starts to degrade at a rate of 6dB per octave. R2 could optionally have an even larger resistance value, with back-to-back diodes connected across the resistor (i.e. two diodes, one with each polarity in parallel with R2, as shown in Figure 2a).

The time constant of the low pass filter R5,C5 should conveniently be chosen to give a sideband frequency for the further negative DC feedback path that is a little lower than that defined by R2,C3 and C4, thereby to ensure the lowest possible sideband frequency and the fastest possible settling time after switch-on.

In practice, packaged CMOS gates have input circuits providing protection against electrostatic discharge (ESSD). Such gates may have insufficiently high input impedance for use in an anti-jitter circuit of the kind described with reference to Figure 10 due to a relatively high sideband frequency. In a CMOS IC, implementation of such protection circuity is not needed on the chip and for packaged gates an additional FET or complementary FET pair may be used to provide simple

high impedance input buffering.

Particularly advantageous aspects of the described exemplary embodiments include:

1. An input source having approximately constant amplitude. It is also desirable, but not essential, that the input waveform should have a risetime no longer than about one tenth of an average period of the input waveform. Circuit performance in practice is then found to be improved.

2. An input capacitor C1 (or pair of input capacitors C1 and C2) can be used to form an input charge packet of substantially constant charge value when switched at one terminal by the aforesaid input signal.

3. An integrator capacitor can be used that is charged by constant charge packets at the input frequency rate, and

4. permanently discharged by a controlled discharge current source or sink. The discharge device can be almost any transistor having a reasonably high output impedance for its drain or collector.

5. A low pass filter (typically a single section RC filter) may be connected to form a negative feedback path from the storage capacitor to the control input (gate or base)

of the controlled current source.

6. The negative feedback connection causes a substantially constant mean d.c. level to exist on the storage capacitor. The feedback thus performs the function of d.c. removal so that the storage capacitor, considered as an integrator of the charge and discharge currents, is not affected by d.c. drift.

7. A differential comparator can be used with one input connected to, and responsive to the sawtooth waveform on, the storage capacitor and the other input connected to the mean d.c. level (at the output of the low pass filter).

8. A triggered output circuit as described in the aforementioned publication, can be connected to be triggered only by the low jitter output transition of the comparator. (The low jitter transition occurs on the slower of the two sawtooth waveform slopes).

9. Back to back speedup diodes (D5 to D8) can be connected to form a low impedance path between the input and output of the feedback low pass filter for the case when input phase jumps cause the integrator voltage to jump out of limits set by the number of diodes in series and the typical diodes offset voltages.

10. A frequency doubling input circuit may be provided in which two charge pumps operate alternately on the rising and falling edges of the input waveform and

convey their charge packets via a common path to the storage capacitor.

11. (a). A common gate or common base transistor circuit may be connected in the path between the input capacitor(s) and the storage capacitor, so that better constancy of charge packets in ensured.

(b). A time constant may also be connected to the base to ensure constancy of charge packet size in the short term fluctuations in input signal amplitude. Or the gate of T2 may be connected to the gate of T1.

12. The use of the low pass filter output voltage (which is known function of frequency) to keep the mark space ratio of an output monostable essentially constant for a wide range of input frequencies. A FET can alternatively be connected to the gate of T1 mirror the current of T1 to a current controlled output monostable to achieve the same objective.

CLAIMS

1. An anti-jitter circuit for reducing time jitter in an input pulse train comprising,

an integrator charge storage means,

charging means for deriving from the input pulse train at least one charge packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means, and

discharging means for continuously discharging the integrator charge storage means,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage waveform having a mean d.c. voltage level, and

means for comparing said time varying voltage waveform with said mean d.c. voltage level and deriving an output pulse train as a result of the comparison.

2. An anti-jitter circuit as claimed in claim 1 wherein said discharging means comprises a discharge device having a control input and means defining a negative feedback path between the control input and an output of the integrator charge storage means whereby to maintain said mean d.c. voltage level substantially constant.

3. An anti-jitter circuit as claimed in claim 2 wherein said discharge device is a current source or a current sink.

4. An anti-jitter circuit as claimed in claim 3 wherein said discharge device is a transistor.

5. An anti-jitter circuit is claimed in any one of the claims 2 to 4 wherein said means defining a negative feedback path comprises a low pass filter.

6. An anti-jitter circuit as claimed in claim 5 wherein the negative feedback path is formed by the combination of a resistor and a capacitor.

7. An anti-jitter circuit as claimed in any one of claims 2 to 6 wherein said mean d.c. voltage level is generated at an output of said negative feedback path and said means for comparing comprises a comparator having a first input coupled to the integrator charge storage means and a second input coupled to said output of the negative feedback path.

8. An anti-jitter circuit is claimed in any one of the claims 2 to 7 including a monostable circuit connected to the output of said means for comparing.

9. An anti-jitter circuit as claimed in claim 8 wherein said mean d.c. voltage level is used to control the pulse length of pulses output by the monostable circuit.

10. An anti-jitter circuit as claimed in claim 9 wherein the monostable circuit is a

current-controlled monostable circuit and has a control input coupled to the output of said negative feedback path by a current mirror matched to said discharge device.

11. An anti-jitter circuit as claimed in claim 10 wherein said discharge device and said current mirror are matched transistors.

12. An anti-jitter circuit as claimed in any one of claims 8 to 11 wherein said monostable circuit is triggered whenever a discharge part of the time-varying voltage waveform crosses the mean d.c. level.

13. An anti-jitter circuit as claimed in any one of claims 1 to 12 including frequency doubling means comprising a first said charging means and a second said charging means for deriving charge packets respectively from the rising and falling edges of the input pulse train.

14. An anti-jitter circuit as claimed in any one of claims 1 to 13 including means for maintaining the charge value of the charge packets substantially constant.

15. An anti-jitter circuit as claimed in claim 14 wherein said means for maintaining comprises a further transistor coupled between said charging means and said integrator charge storage means.

16. An anti-jitter circuit as claimed in claim 15 wherein said further transistor is arranged to operate in grounded base mode.

17. An anti-jitter circuit as claimed in claim 16 including averaging means connected to the base of the further transistor.

18. An anti-jitter circuit as claimed in claim 15 wherein said discharging means includes a first field effect transistor operative as a discharge device and said further transistor is a second field effective transistor, and the gate of the first field effect transistor is connected to the gate of the second field effect transistor.

19. An anti-jitter circuit as claimed in any one of claims 2 to 6 wherein said means for comparing comprises inverted gate means having an input coupled to the integrator charge storage means and an output, and including means defining a further negative feedback path between said output of said inverted gate means and said discharging means whereby to establish said mean d.c voltage level as a switching level of said inverted gate means.

20. An anti-jitter circuit as claimed in claim 19 wherein said further negative feedback path is connected between said output of said inverted gate means and said control input of said discharging device.

21. An anti-jitter circuit as claimed in claim 19 or claim 20 wherein said further negative feedback path comprises a low pass filter.

22. An anti-jitter circuit as claimed in claim 21 wherein said low pass filter comprises the combination of a resistor and a capacitor.

23. An anti-jitter circuit as claimed in any one of claims 2 to 6 wherein said means for comparing comprises inverted gate means having an input coupled to the integrator charge storage means and an output, and including a voltage source coupled to the discharging means whereby to establish said mean d.c voltage level as a switching level of said inverted gate means.

24. An anti-jitter circuit as claimed in claim 23 wherein said voltage source is connected between said output of said inverted gate means and said control input of said discharging device.

25. An anti-jitter circuit as claimed in any one of claims 2 to 24 including means providing a low impedance path between the input and the output of the negative feedback path.

26. An anti-jitter circuit as claimed in claim 25 wherein said low impedance path is formed by diodes connected back-to-back.

27. An anti-jitter circuit as claimed in any one of the claims 1 to 26 wherein the or each said charging means is a charge pump.

28. An anti-jitter circuit substantially as herein described with reference to Figures 2 to 10 of the accompanying drawings.

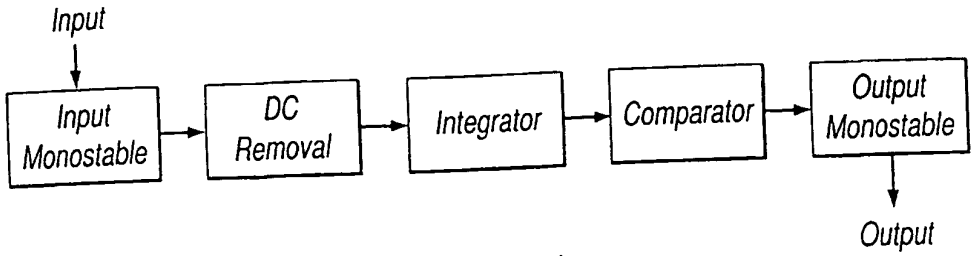


Fig.1(a)

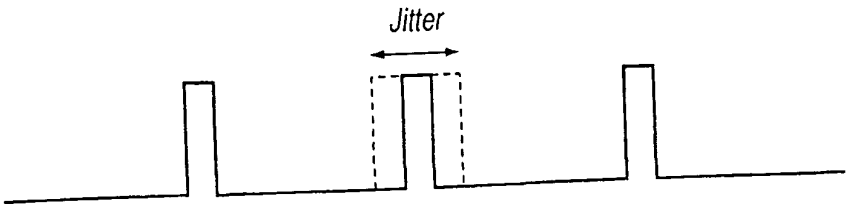


Fig.1(b)

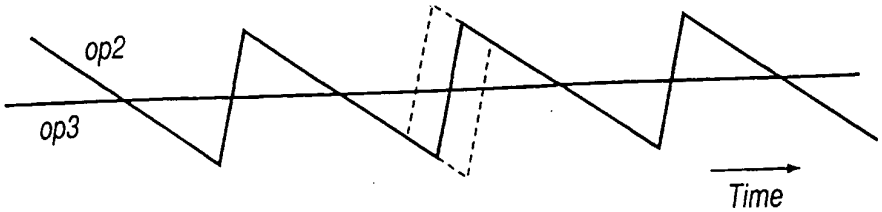
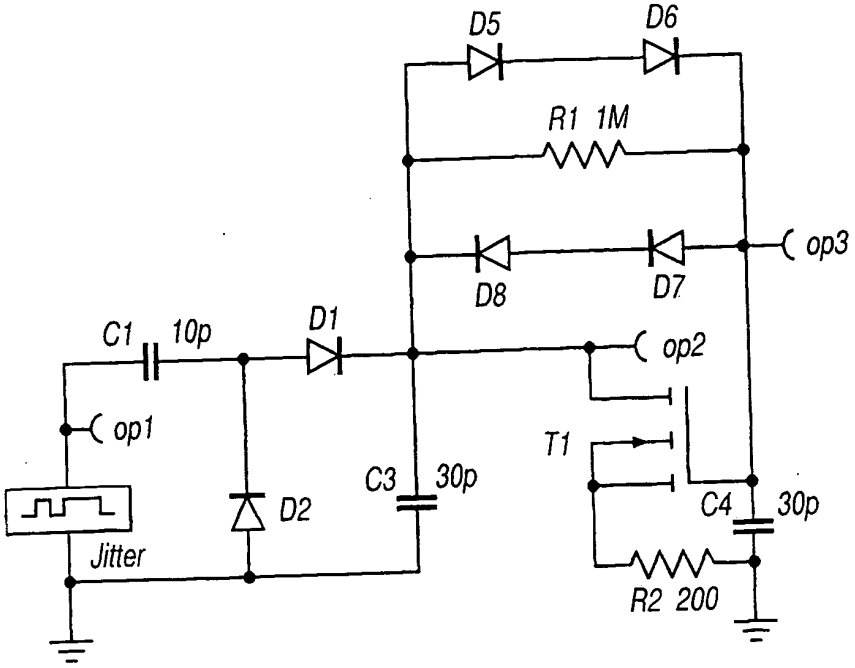


Fig.1(c)

Fig.1 Anti Jitter Circuit Principle:-

(a) Basic Block Diagram
(b) Input with jitter on central pulse
(c) Integrator output (op2) and Comparator switching level (op3)



T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of 150 degrees
= Time Jitter of 1 usec in 2.4usec at 1/3 rate

Fig.2(a)

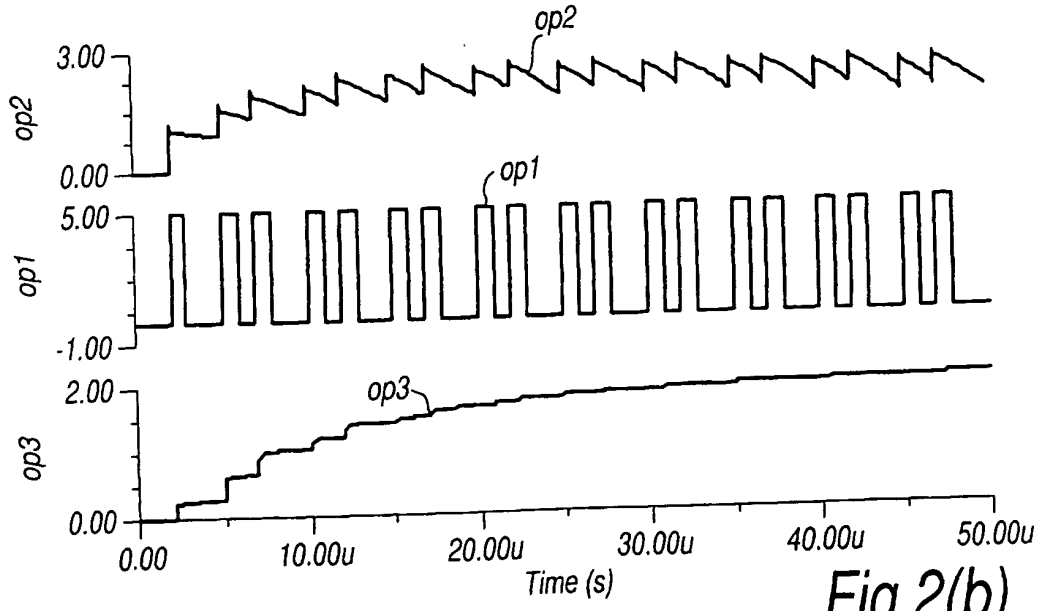


Fig.2(b)

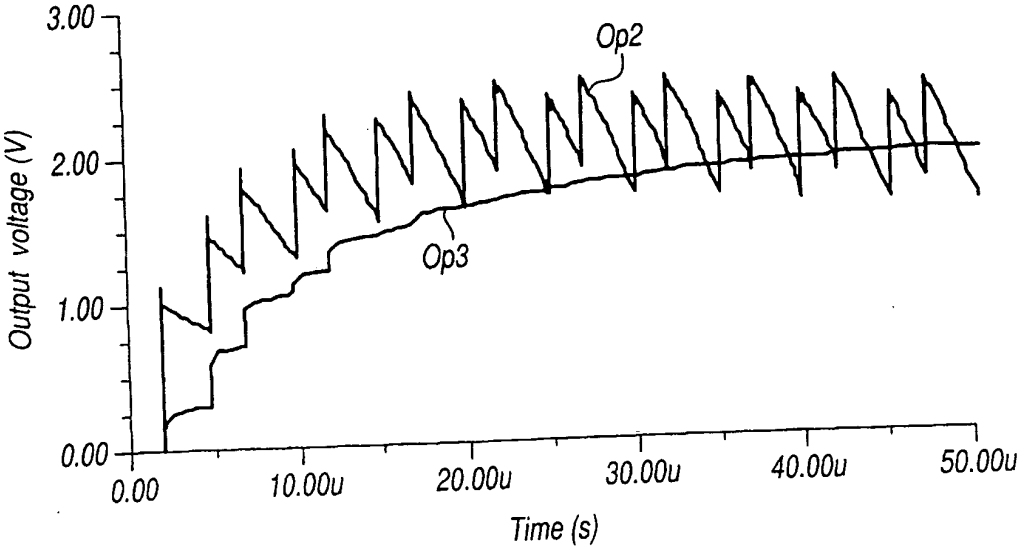

3.00
2.00
1.00
0.00
Output voltage (V)
Op2
Op3
0.00
10.00u
20.00u
30.00u
40.00u
50.00u
Time (s)

Fig.2(c)

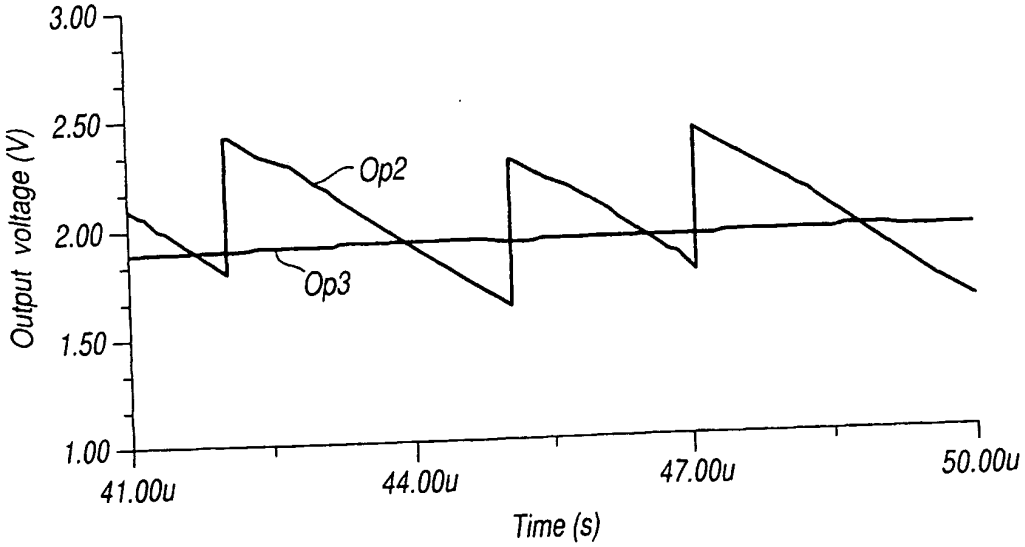

3.00
2.50
2.00
1.50
1.00
Output voltage (V)
Op2
Op3
41.00u
44.00u
47.00u
50.00u
Time (s)

Fig.2(d)

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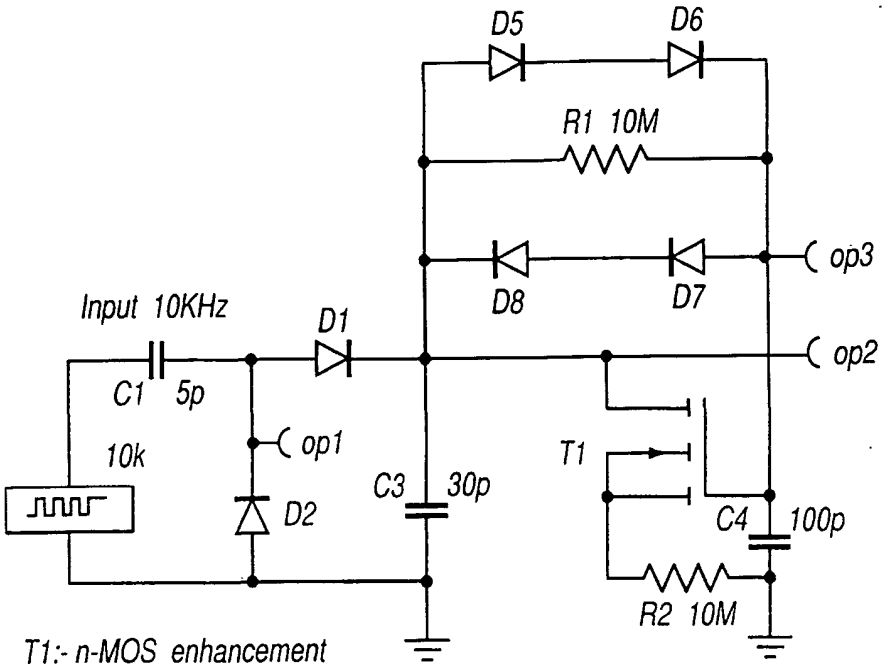


T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Fig.3(a)

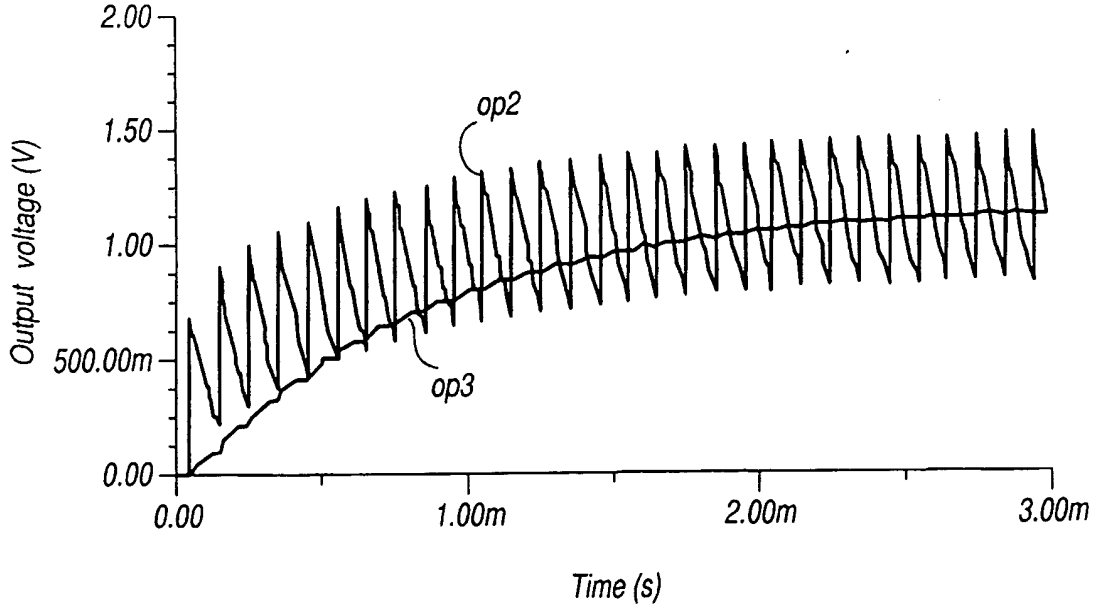
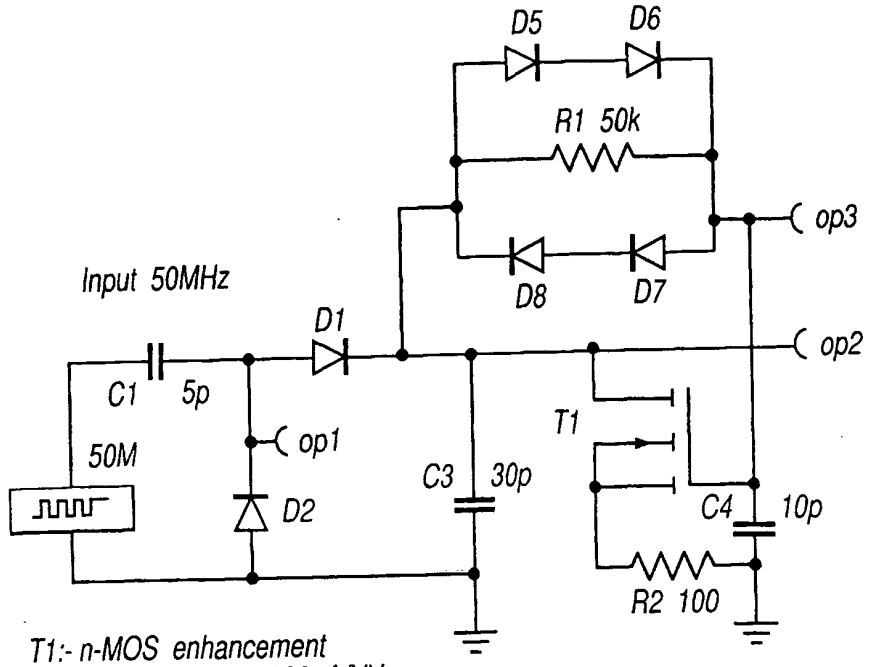


Fig.3(b)



T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Fig.4(a)

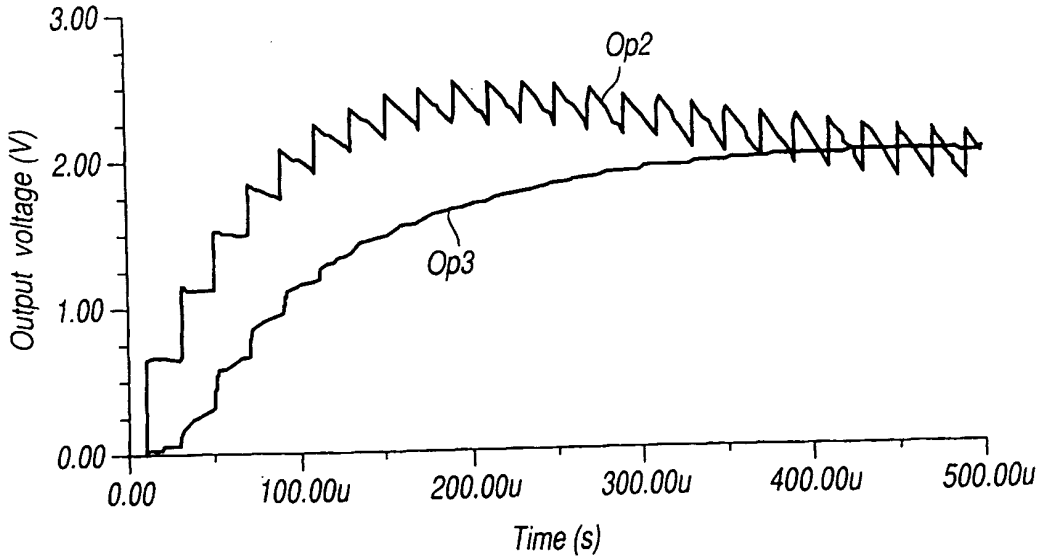
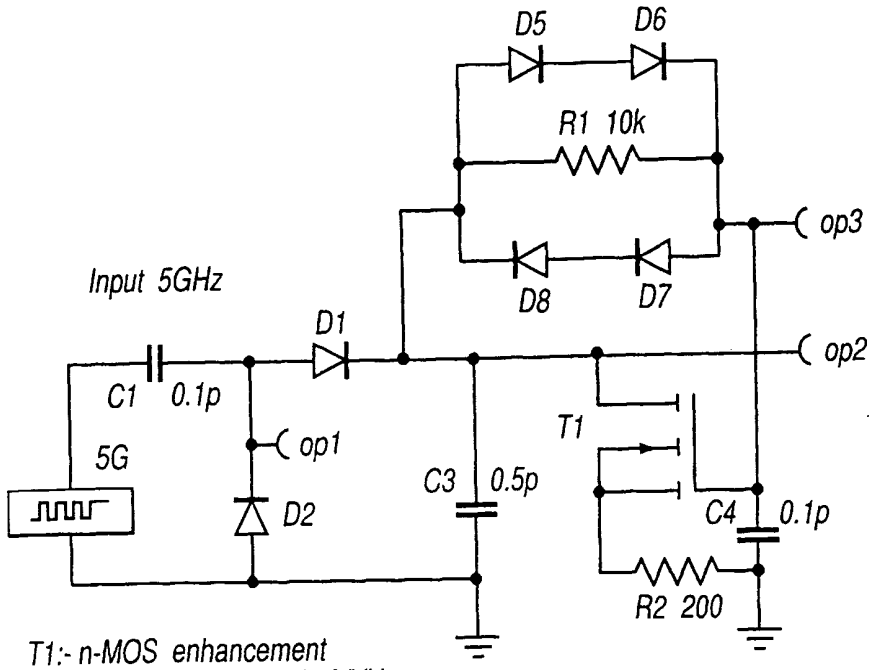


Fig.4(b)



T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Fig.5(a)

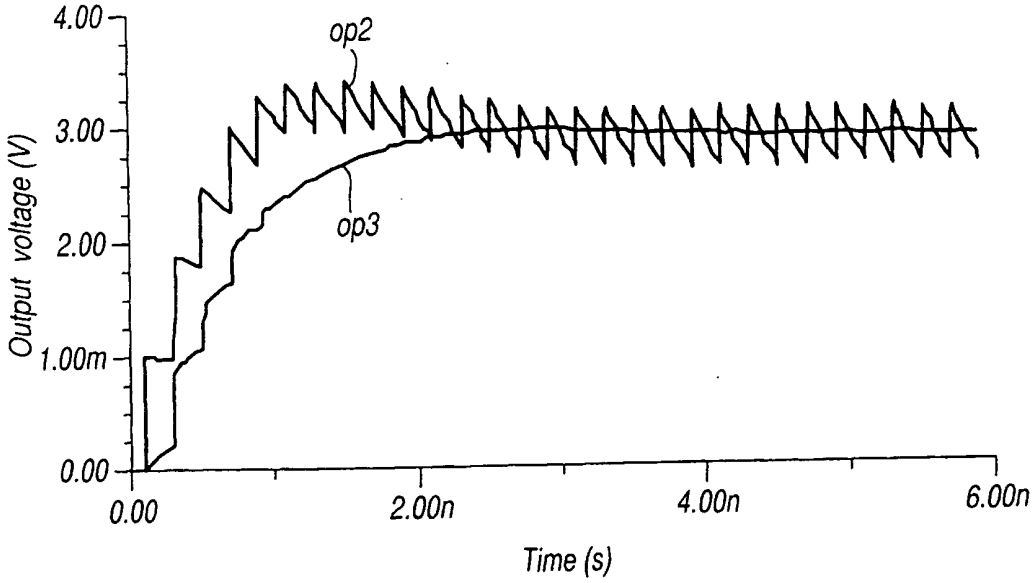


Fig.5(b)

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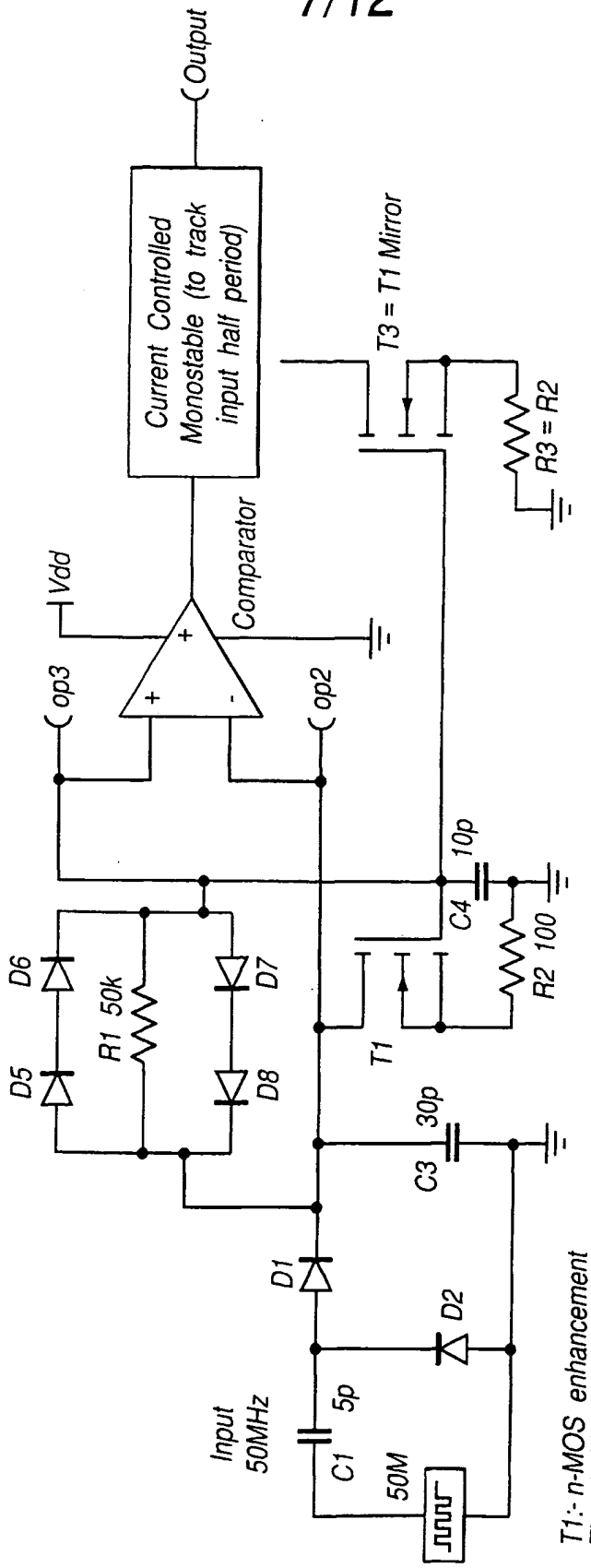

Fig.6

AAJC with Comparator and input-tracking Output Monostable

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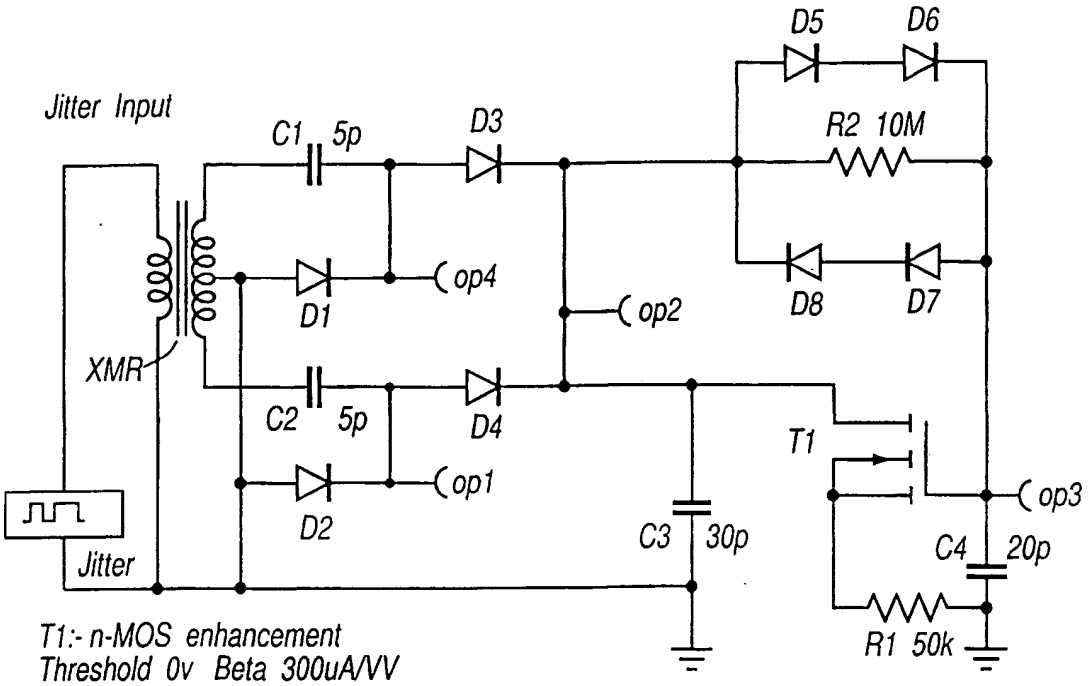


T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of 150 degrees
= Time Jitter of 1 usec in 2.4 usec at 1/3 rate

Fig.7(a)

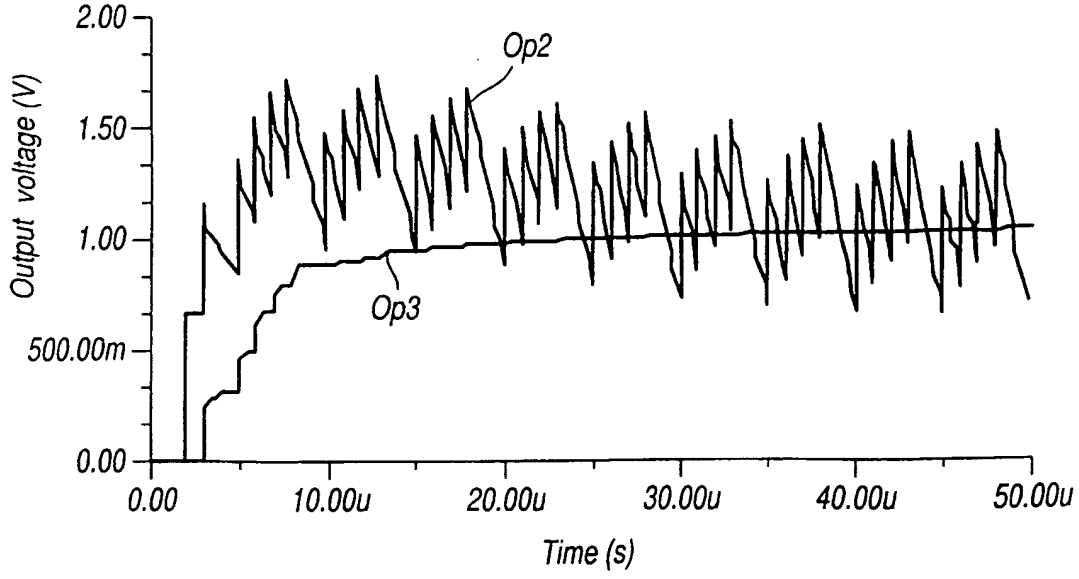


Fig.7(b)

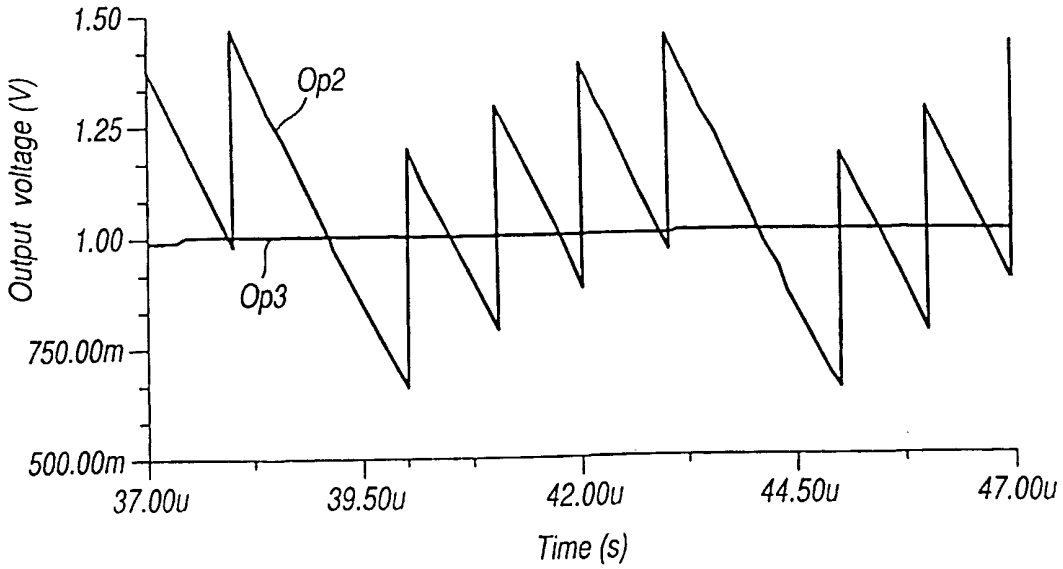
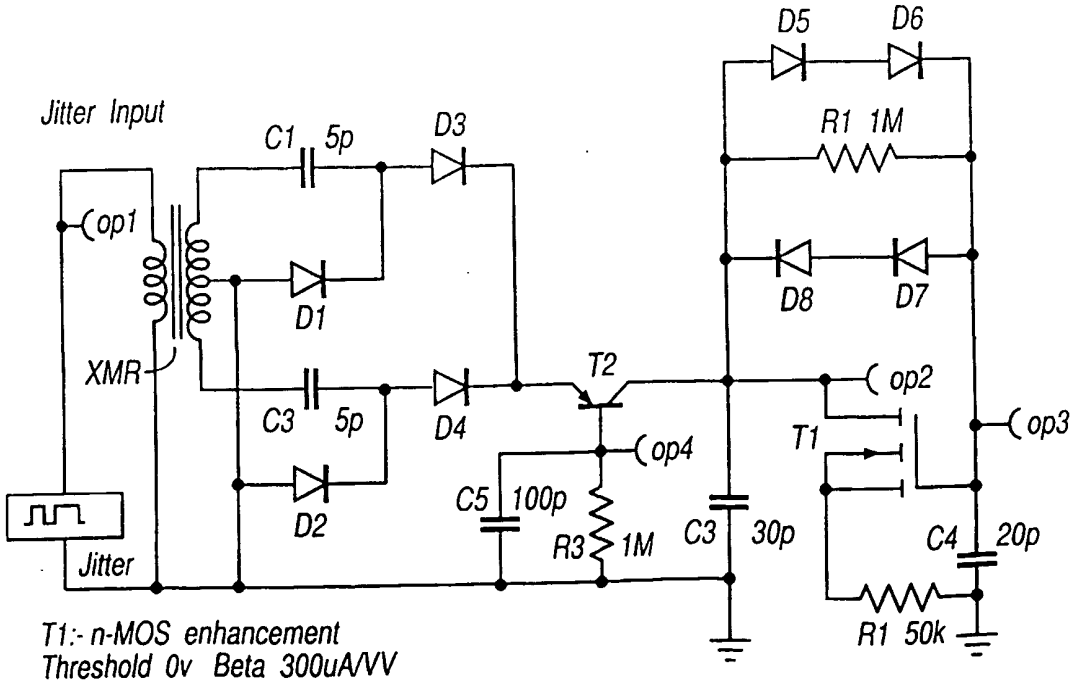


Fig.7(c)



T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of 150 degrees
= Time Jitter of 1 usec in 2.4 usec at 1/3 rate

Fig.8(a)

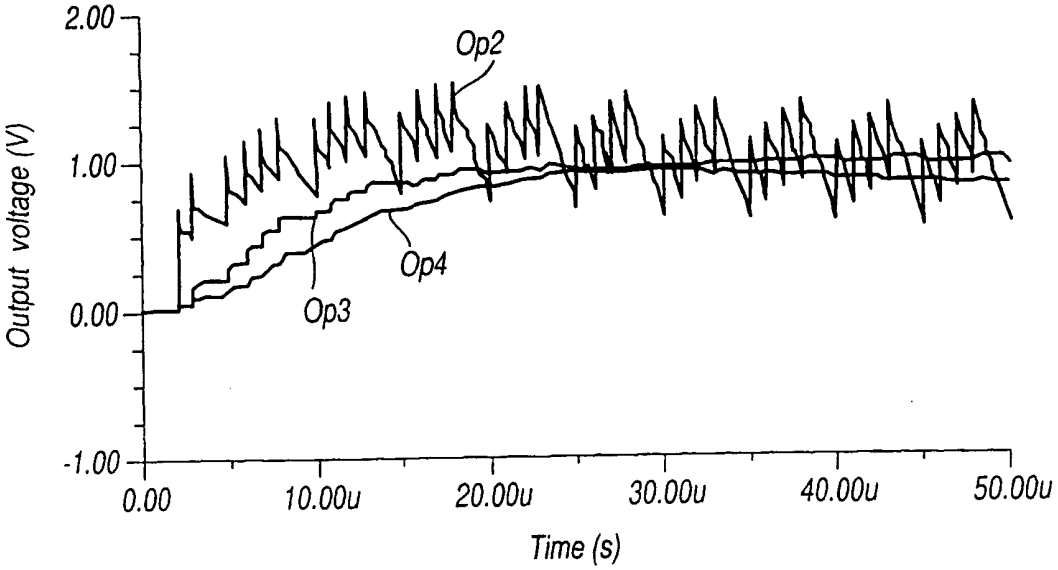

2.00
1.00
0.00
-1.00
Output voltage (V)
Op2
Op4
Op3
0.00
10.00u
20.00u
30.00u
40.00u
50.00u
Time (s)

Fig.8(b)

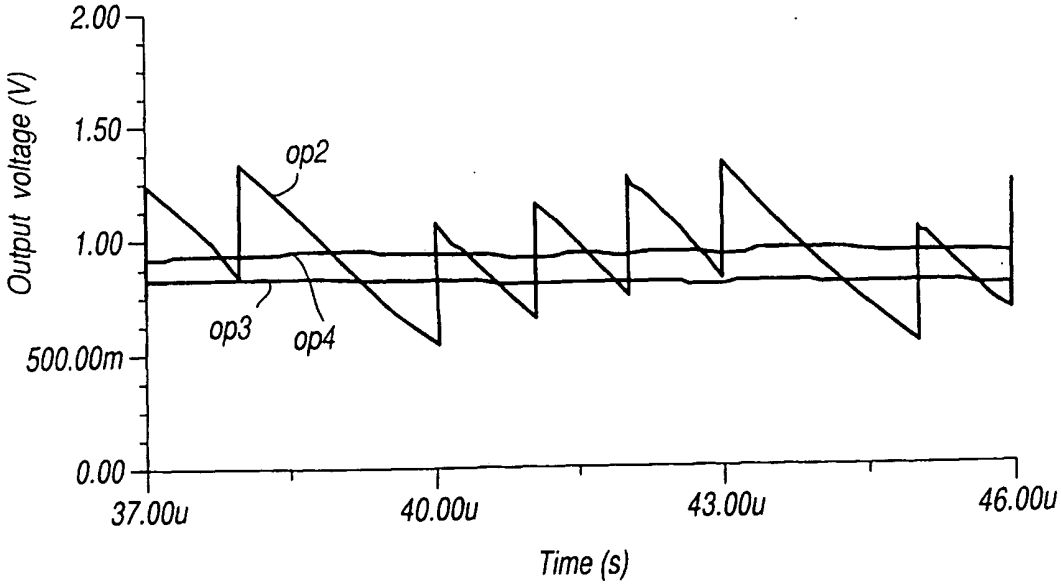
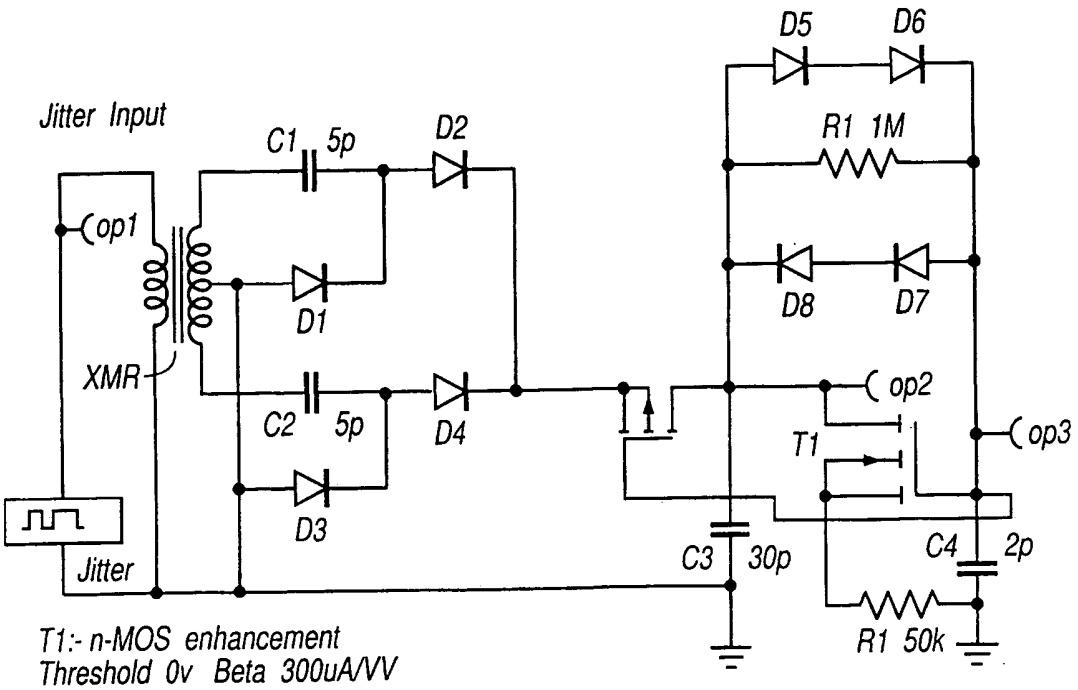

2.00
1.50
1.00
500.00m
0.00
Output voltage (V)
op2
op3
op4
37.00u
40.00u
43.00u
46.00u
Time (s)

Fig.8(c)



T1:- n-MOS enhancement
Threshold 0v Beta 300uA/VV

op2 and op3 to differential comparator

Mean Fin = 417kHz and 1/3 rate phase jumps of 300 degrees
= Time Jitter of 1 usec in 2.4 usec at 1/3 rate

Fig.9(a)

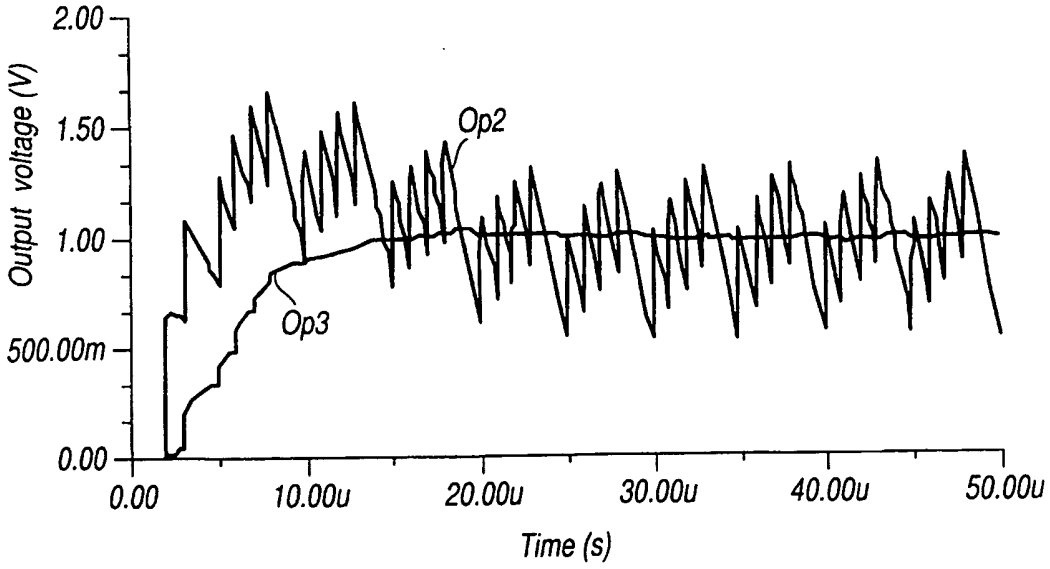


Fig.9(b)

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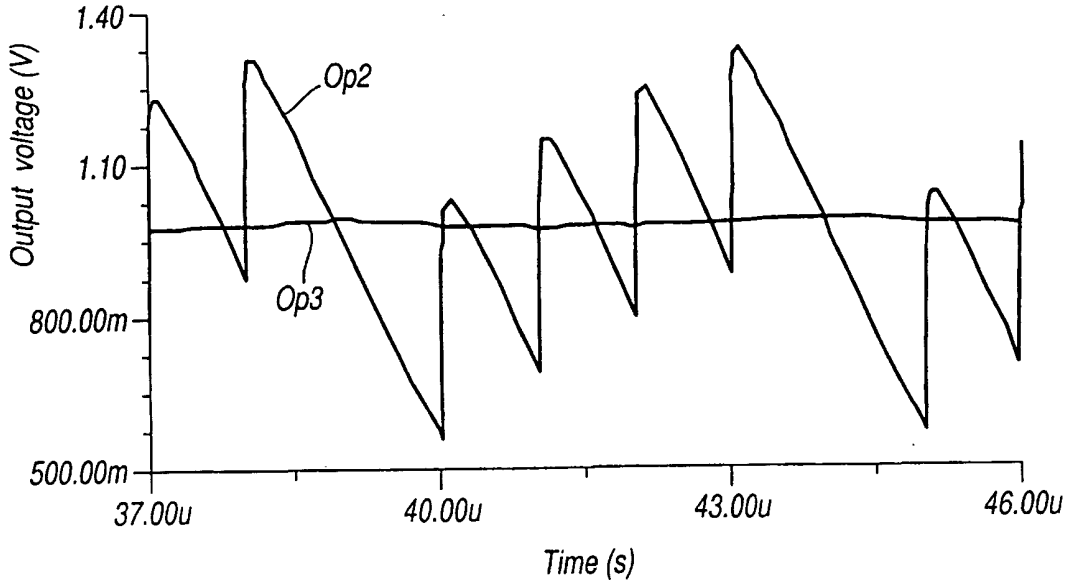

Fig.9(c)

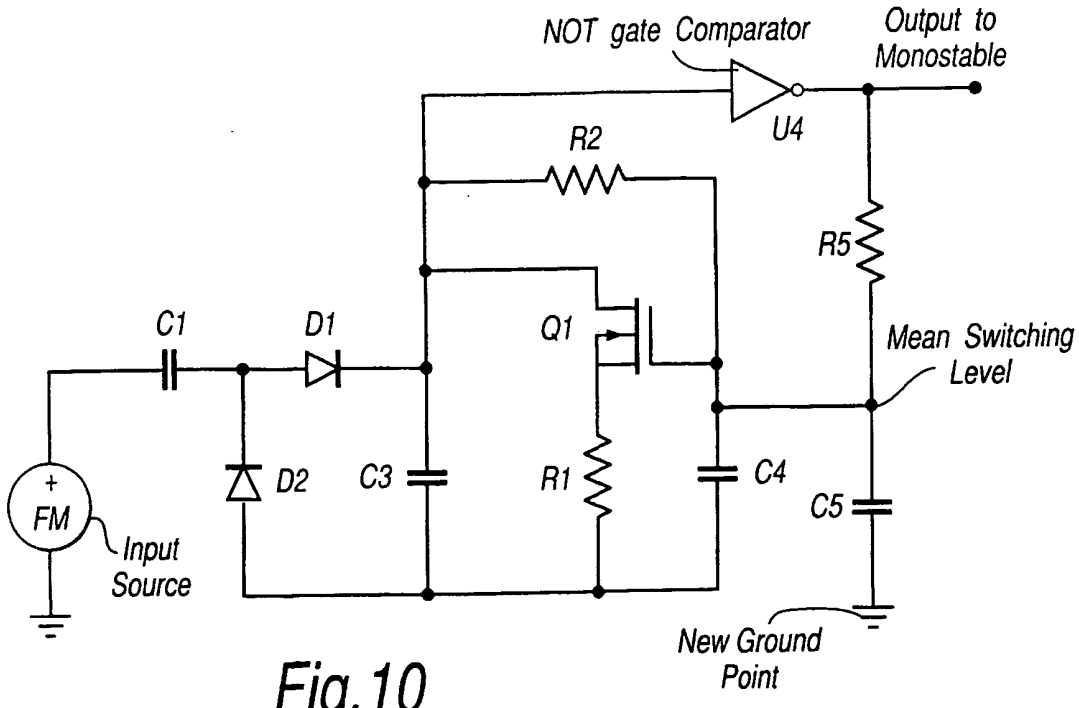

Fig.10